

REMARKS

The specification and claims 1 and 11 have been amended, claims 19-27 have been canceled, and claims 28-36 have been added. As such, claims 1-18 and 28-36 are currently pending in the case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Section 102 Rejections

Claims 1-9, 11-17, 19-24, and 27 were rejected under 35 U.S.C. § 102(c) as being anticipated by U.S. Patent No. 6,444,584 to Hsiao et al. (hereinafter referred to as "Hsiao"). Claims 19-27 have been canceled rendering rejection thereto moot. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. Of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987), MPEP 2131. Hsiao does not teach or suggest all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

Hsiao does not disclose etching a stack of layers within a single etch chamber, wherein the stack of layers comprises an antireflective layer and a nitride layer arranged beneath and in contact with the antireflective layer. Amended claim 1 recites in part: "[a] method for processing a semiconductor topography, comprising: etching a stack of layers within a single etch chamber, wherein the stack of layers comprises: an anti-reflective layer; a nitride arranged beneath and in contact with the antireflective layer ..." Support for such a limitation may be found, for example, in Figs. 3-5 and corresponding text of the present specification. Hsiao specifically teaches etching a silicon/dielectric/silicon stack of layers to form, for example, a polysilicon capacitor or a gate electrode for a field effect transistor. Although Hsiao teaches etching an antireflective layer prior to etching the stack of layers, there is no teaching or suggestion within Hsiao of etching a stack of layers having an antireflective layer arranged upon and in contact with a nitride layer as in the presently claimed case. Consequently, Hsiao does not anticipate limitations of independent claim 1 or claims dependent therefrom. Accordingly, Applicants respectfully request removal of this rejection.

Section 103 Rejections

Claims 10, 25, and 26 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsiao. Claim 18 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Hsiao in view of U.S. Patent No. 6,117,786 to Khajehnouri et al. (hereinafter referred to as "Khajehnouri"). As noted above, claims 25 and 26 have been canceled rendering rejection thereto moot. To establish a *prima facie* obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03. Neither Hsiao nor Khajehnouri teaches or suggests all limitations of the currently pending claims, some distinctive limitations of which are set forth in more detail below.

Neither Hsiao nor Khajehnouri teaches or suggests etching a stack of layers within a single etch chamber, wherein the stack of layers comprises an antireflective layer and a nitride layer arranged beneath and in contact with the antireflective layer. This is the same limitation of claim 1 argued above in regard to the § 102(e) rejection. As noted above, Hsiao does not provide any teaching or suggestion of etching a stack of layers having an antireflective layer arranged upon and in contact with a nitride layer. Furthermore, there is no motivation for one skilled in the art to etch a stack of layers having an antireflective layer arranged upon and in contact with a nitride layer based on the teaching of Hsiao, since Hsiao only discusses using the single plasma etching process described therein to etch silicon/dielectric/silicon stacks of layers. Such a lack of teaching and motivation cannot be overcome with the teachings of Khajehnouri, since Khajehnouri only discusses etching silicon oxide with the etch chemistry described therein. Consequently, claim 1 is asserted to be patentably distinct over the cited art.

None of the cited art teaches or suggests etching an antireflective layer in a low-density plasma etch chamber. Amended claim 11 recites in part: "[a] method for processing a semiconductor topography, comprising: etching an anti-reflective layer in a low density plasma etch chamber ..." Support for such a limitation may be found, for example, on page 12, lines 12-18:

Regardless of the fabrication process and etch chemistry used, anti-reflective layer 30, cap layer 28, and device layer 26 are preferably etched within the same chamber ... For example, the etch tool may be a plasma etch tool with a plasma density between approximately 2.0×10^9 molecules/cm³ and approximately 2.0×10^{11} molecules/cm³. Such a plasma density range may be representative of a range sometimes referred to as a "low-density plasma."

Hsiao fails to mention the type of etch chamber the antireflective and silicon/dielectric/silicon stack of layers are etched in, much less an etch chamber configured to generate a low-density plasma. Without any teaching or suggestion of such a limitation, there is no motivation within Hsiao to teach the limitations of claim 11. Khajehnouri specifically teaches in column 2, lines 3-4 etching with a medium density plasma reactor and, therefore, does not teach or suggest etching with a low density plasma reactor. Consequently, Khajehnouri cannot be combined with Hsiao to teach the limitations of claim 11. Furthermore, even if Khajehnouri taught etching in a low density plasma reactor, for the sake of argument, there is no motivation to combine Khajehnouri with Hsiao since they teach etching different materials.

For at least the reasons stated above, neither Hsiao nor Khajehnouri teaches, suggests, or provides motivation to teach the limitations of claims 1 or 11. Therefore, claims 1 and 11, as well as claims dependent therefrom, are asserted to be patentably distinct over the cited art. Accordingly, Applicants respectfully request removal of this rejection.

Patentability of the Added Claims

The present Amendment adds claims 28-36. Claim 28, which is dependent upon claim 11, is patentably distinct over the cited art for at least the same reasons as that claim. As will be set forth in more detail below, claims 29-36 are also patentably distinct over the cited art.

None of the cited art teaches or suggests etching a stack of layers comprising an antireflective layer and a silicon nitride layer in a single etch chamber with a sequence of different etch chemistries. Added claim 29 recites:

A method for processing a semiconductor topography, comprising etching a stack of layers in a single etch chamber with a sequence of different etch chemistries, wherein the step of etching the stack of layers comprises: etching an antireflective layer with a first etch chemistry comprising a noble gas heavier than helium; and etching a silicon nitride layer with a second etch chemistry different than the first etch chemistry.

Support for the limitations of added claim 29 may be found, for example, on page 11, lines 28-29, of the present specification, "... the etch processes of Figs. 3-5 may include different etch chemistries such that each etch process is distinct from one another." Hsiao specifically teaches etching the antireflective and silicon/dielectric/silicon stack of layers described therein "... employing a single plasma etch method employing a single etchant gas composition ..." (column 3, lines 30-31). Khajehnouri fails to discuss etching

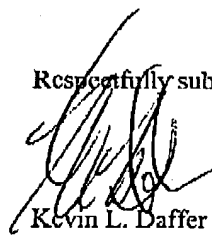
multiple layers and using multiple etch chemistries, much less etching antireflective and nitride layers with multiple etch chemistries. Consequently, Hsiao and Khajehnouri, taken alone or in combination, fail to teach the limitations of added claim 29 or claims dependent therefrom. Accordingly, allowance of claims 28-36 is respectfully requested.

CONCLUSION

This response constitutes a complete response to all issues raised in the Office Action mailed February 3, 2004. In view of the remarks traversing the rejections, Applicants assert that pending claims 1-18 and 28-36 are in condition for allowance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment; however, the Commissioner is authorized to charge any additional fees, which may be required, or credit any overpayment, to Conley Rose, P.C. Deposit Account No. 03-2769/5298-06900.

Respectfully submitted,



Kevin L. Daffer
Reg. No. 34,146
Attorney for Applicants

Conley Rose, P.C.
P.O. Box 684908
Austin, TX 78768-4908
Ph: (512) 476-1400
Date: May 3, 2004
MHL